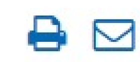
Intel and National Science Foundation Lead Research on Wafer- or Panel-Scale Heterogeneous Integration



Highlights

- The National Science Foundation and Intel will collaborate on the NSF's 2025 ASCENT program on wafer-scale or panel-scale heterogeneous integration in advanced packaging.
- Through research collaboration with universities, Intel will explore how to overcome I/O performance walls to meet AI compute demands.
- Miniaturizing the footprint of a data center rack down to the scale of panel-size advanced packaging will optimize the energy needed for communication.

The National Science Foundation (NSF) and Intel will collaborate on the NSF's 2025 Addressing Systems Challenges through Engineering Teams (ASCENT) program, and work together on research focused on wafer-scale or panel-scale heterogeneous integration (HI) of innovative semiconductor systems through advanced packaging.

Through research collaboration with universities, Intel will explore how to increase compute integration to overcome industry-wide input/output (I/O) performance walls using wafer- or panel-scale HI to ultimately provide more efficient, sustainable growth for artificial intelligence (AI) systems. This critical research will address the issues associated with today's rapid AI model growth, which is fueling an exponential demand for compute yet performance is not scaling in tandem due to memory and I/O bandwidth and power barriers.

One of the challenges researchers will tackle in the program is how to miniaturize the footprint of a data center rack down to the scale of panel-size advanced packaging and optimize the energy required for communication. The I/O energy efficiency cost to move data around in large data center networks is as much as two orders of magnitude greater compared to moving data within a compute package.

Researchers will investigate building semiconductor systems with wafer-size (up to 300 mm diameter) or panel-size (up to 500 mm by 500 mm) materials while densely integrating components to maximize system performance and efficiency. Wafer-scale integration involves manufacturing integrated circuits on a wafer while reserving a significant portion of the wafer for the compute system. By extending the integration to panels such as glass, panel-scale HI provides more than 3x the area compared to wafer scale.

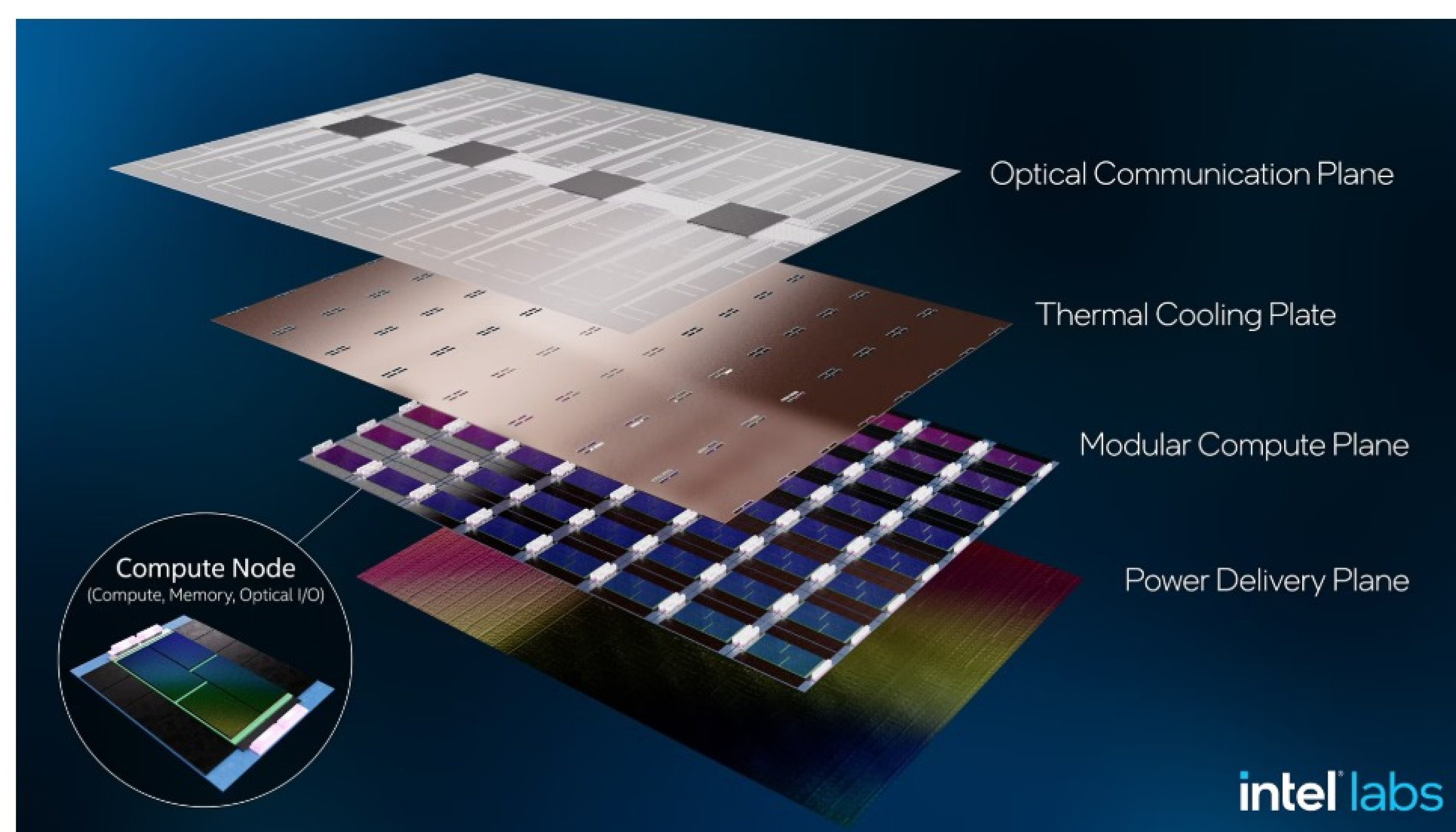


Figure 1. Concept illustration of a panel-scale compute system and assembly with four primary panel-sized layers. These layers feature an optical communication plane, thermal cooling plate, modular compute plane, and power delivery plane. The subsystem compute node includes compute, memory, and optical I/O integrated circuits (ICs).

A panel-scale HI computer system may involve 2.5D or 3D planes for compute, memory, I/O, thermals, and power delivery. A complete system architecture involving communications, and compute integrates various technologies to optimize system performance while providing modular assemblies for flexibility.

Examples of potential research areas include:

- Modular sub-microsystems (compute, memory, and communication) and ICs, fine-pitch out-of-plane optical couplers, optical backplanes and optical switch integration, system power delivery, and thermal solutions.
- Optical and electrical communication fabrics capable of panel edge to panel edge reach without active repeaters, low-loss waveguides, optical switches, temperature resilient photonics, and ultra-low energy I/O.
- Dynamically programmable fabrics, mesh networks, hierarchical networks, network protocols to optimize bandwidth/latency, and algorithms for libraries of collective operations.
- System architecture designs featuring redundant and resilient circuit techniques.
- Test strategies for improved yield and methods for system resiliency.

Among the benefits of the research, panel-scale systems are expected to increase compute and memory density of the number of chips placed in each area compared to current packaging and printed circuit board technologies. This smaller footprint leads to a reduction in system communication energy as well as increased bandwidth/latency efficiency compared to current data center optical networks. Panel-scale system performance gains are expected to increase compared to today's performance for targeted AI, machine learning, and high-performance computing workloads. Through panel-scale system and software co-innovation, the research also will explore new network protocols to optimize bandwidth/latency of a dynamically programmable fabric, and new algorithms for libraries of collective operations to provide a foundation of topology aware AI workloads.

Learn more about the NSF ASCENT program solicitation.

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