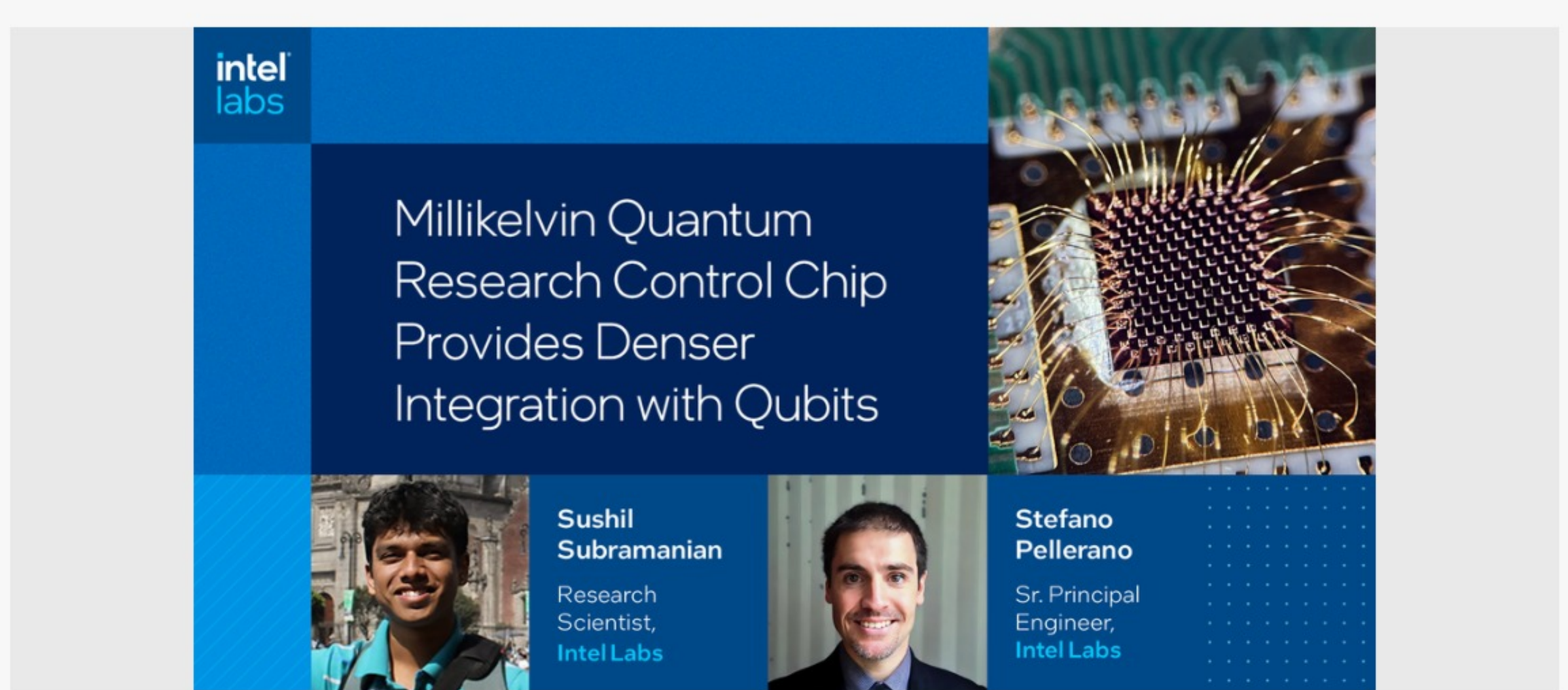


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Intel's Millikelvin Quantum Research Control Chip Provides Denser Integration with Qubits



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Sushil Subramanian is a research scientist at Intel where he works on integrated circuits and systems for qubit control in quantum computers. Co-author Stefano Pellerano is a senior principal engineer and lab director of the RF and Mixed-Signal Circuits Lab where he leads the research and development effort on cryogenic electronics for qubit control.

Highlights

- Intel's millikelvin quantum research control chip, code-named Pando Tree, establishes Intel as the first semiconductor manufacturer to demonstrate the distribution of cryogenic silicon spin qubit control electronics inside the dilution refrigerator at different temperature stages.
- Using both control chips, Horse Ridge II at the 4 kelvin stage and Pando Tree at the 10 to 20 millikelvin stage, achieves a more efficient overall solution for large-scale silicon qubit control.
- Deploying traditional CMOS circuit capability at the millikelvin stage of the dilution refrigerator will enable quantum scaling to millions of qubits in the future.

Large-scale silicon qubit control requires closer integration of control electronics to qubits at the millikelvin stage of the dilution refrigerator to address the wiring bottleneck limiting the scaling of quantum computing. Based on newly released research at the [2024 IEEE Symposium on VLSI Technology & Circuits](#), Intel's millikelvin cryogenic control chip, code-named Pando Tree, establishes the company as the first semiconductor manufacturer to demonstrate the distribution of cryogenic silicon spin qubit control electronics inside the dilution refrigerator at different temperature stages. Using both control chips, Horse Ridge II at the 4 kelvin stage and Pando Tree at the 10 to 20 millikelvin stage, achieves a more efficient overall solution for large-scale silicon qubit control. Deploying traditional complementary metal oxide semiconductor (CMOS) circuit capability at the millikelvin stage will enable quantum scaling to millions of qubits in the future.



Figure 1. Intel's millikelvin control chip, Pando Tree, is closer to the spin qubit chip.

Serving as a demultiplexer chip, Pando Tree is integrated with a Tunnel Falls spin qubit research chip on the same printed circuit board (PCB) in the millikelvin stage of the refrigerator. The Horse Ridge II controller generates a fast sequence of the required control voltages for the qubits using a single signal line and nine digital control signals to program Pando Tree. The demultiplexer chip then takes each voltage in the input sequence and delivers it to multiple qubit chip control terminals based on the address information provided by Horse Ridge II. Pando Tree can deliver both constant voltage bias and high-speed voltage pulsing for up to 64 qubit terminals, which is the largest interconnect demultiplexing capability demonstrated to date in millikelvin control electronics.

Pando Tree features unique control capabilities compared to state-of-the-art quantum control chips, such as providing both precise constant voltages to optimize qubit performance and fast voltage pulses for qubit control. Moreover, these pulses can be applied continuously for complex algorithms and simultaneously to multiple control gates. The latter is particularly critical in counteracting signal crosstalk between the intricate wiring connecting individual qubits, improving overall control fidelity.

Pando Tree is a key step in addressing the quantum computing interconnect bottleneck. Quantum chips are stored in low, cryogenic temperatures in the dilution refrigerator while traditional control electronics that control the qubits operate at room temperature. Getting the control electronics to operate at high fidelity at cryogenic temperatures is important to overcoming the wiring bottleneck. Pando Tree enables a denser level of integration between the controller and the qubit chip.

Steps to Addressing the Interconnect Bottleneck

In 2020, Intel took the first step toward addressing the interconnect challenge with the introduction of Horse Ridge, a cryogenic control chip for qubits implemented using Intel® 22nm low-power FinFET technology (22FFL). A second generation of the chip was introduced later that same year. Horse Ridge II brought key control functions for quantum computer operation into the 4 kelvin stage in the cryogenic refrigerator to streamline the complexity of control wiring for quantum systems.

The original Horse Ridge chip simplified the need for multiple racks of equipment and thousands of wires running into and out of the refrigerator to operate the quantum machine. Intel replaced these bulky instruments with a highly integrated system-on-chip (SoC) that simplifies system design and uses sophisticated signal processing techniques to accelerate setup time, improve qubit performance, and enable the engineering team to efficiently scale the quantum system to larger qubit counts.

While Intel has already demonstrated control using 300 kelvin room temperature instruments and the 4 kelvin Horse Ridge II cryogenic control chip, the constraints from cabling, power, and noise have remained a bottleneck for large qubit systems. Even now, a wiring bottleneck still exists between the 4 kelvin and millikelvin stages of the refrigerator.

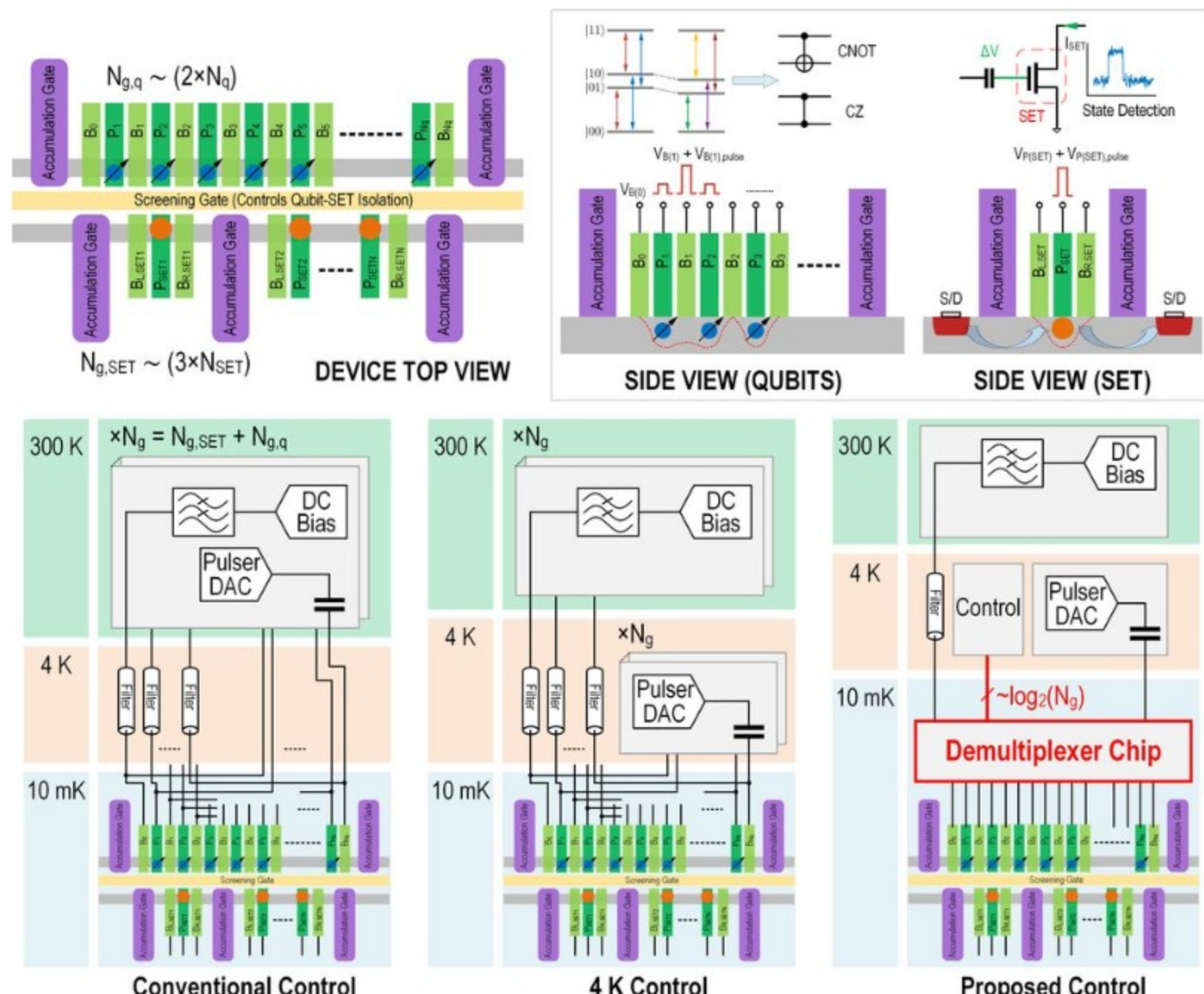


Figure 2. Qubit device with applications of pulsing operations. Proposed 4 kelvin and millikelvin control compared to the conventional control, and Intel's 300 kelvin (room temperature) and 4 kelvin control.

Spin qubits in quantum computers operate in the millikelvin temperature range, which is one thousandth of a kelvin – just a fraction of a degree above absolute zero. Pando Tree gets even closer than Horse Ridge II to the silicon spin qubit chip, deeper down in the refrigerator at a lower temperature of 10 to 20 millikelvins. Even if the number of qubit terminals to control remains the same, having Pando Tree at the millikelvin stage of the dilution refrigerator physically close to the qubit chip enables the use of high-density interconnects from control and qubit chip integration on the same package.

Typically, controlling N qubits would require in the order of N individual signals. With its demultiplexing capability, Pando Tree only requires approximately log(N) input signals to control N qubits. For example, to control one million qubits, more than one million cables would be required. However, using demultiplexing capabilities similar to those implemented in Pando Tree would reduce it to only approximately 20 cables. It is important to note that the interface between Pando Tree and the million qubits would still require more than one million interconnects, but since Pando Tree can operate at millikelvin temperatures next to the qubit chip, the two chips can be co-packaged and advanced packaging interconnect technologies can be leveraged for scaling. This is similar to a modern 3D NAND flash memory stacked vertically in multiple layers — it has one billion bytes that interface using dense interconnects with processors as a self-contained system but requires only 100 input/output pins.

Future Packaging

Although Intel packaging technology was not used for the experimental results, the Pando Tree control chip is designed to be fully compatible with standard Intel Foundry Flip Chip Ball Grid Array 2D (FCBGA 2D) and other advanced packaging technologies for future scaling. By operating in the same millikelvin stage as the qubit chip, Pando Tree can be co-packaged with the qubit chip. In the future, this will allow the millions of interconnect wires required between Pando Tree and the qubit chip to be implemented using the latest Intel Foundry Foveros 2.5D and 3D packaging technologies instead of the PCB traces currently being used.

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